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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,042	07/08/2003	Valeriy Sukharev	03-0509	3892

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,042	SUKHAREV ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/18/06 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. Patent No. 6,334,249 B2) in view of Hsu et al. (U.S. Patent No. 6,143,645) and further in view of Wong (US 2004/0087148 A1).

In re claims 1, 3 and 6, Hsu (esp. Figs. M-2C) disclose a semiconductor device and method of forming the same comprising:

copper deposits (200, column 5, line 35);

an intermediate liner layer (205) comprising tantalum nitride (column 10, line 50); and

an interconnect liner layer (220) comprising aluminum-copper alloy (column 10, line 34), wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper deposit to form an alloy at any time while the method is performed; and

an upper copper layer (column 5, lines 53-55), wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper ol copper deposit to form an alloy at any time while the method is performed (as a result of the presence of the TaN layer as described in Applicant's specification.)

Hsu ('249) does not expressly disclose the use of CMP, but does disclose the upper layer having a degree of planarity (column 5, lines 18-19). Hsu ('645) discloses the use of CMP for damascene devices such as this (column 6, lines 8-10). CMP is also well-known method of forming planar layers in the art and it would have been obvious for one skilled in the art at the time of the invention to use such a process, for the purpose, for example, of producing more uniform devices.

Hsu ('249) does not expressly disclose the formation of a trench structure in combination with a via structure, but does disclose the use of the invention in a damascene structure (column 8, lines 50-51). Hsu ('645) further describes the damascene processing structure as comprising a trench (upper) portion as well as a via (lower) portion (column 5, lines 61-67), where "deeper holes" (vias) are formed. Damascene processes that produce these trench and via structures are also well known

in the art. Therefore, though not expressly disclosed by Hsu ('249), it would have been obvious for one skilled in the art at the time of the invention to form the interconnect liner layer along a trench and via sidewalls, because such a structure is a product of damascene interconnect technology and such is disclosed by the prior art of record.

Although Hsu in view of Hsu discloses polishing the copper interconnect structure by CMP, neither of said references show the copper interconnect structure in a larger scale such that adjacent dielectric layers are shown to be at the same planar level as the interconnect. Wong (e.g., Figs. 8, 9) discloses the process and resulting product of planarizing a copper deposit to the level of an upper dielectric layer (22). It would have been obvious to one skilled in the art at the time of the invention to polish the copper deposit of Hsu/Hsu back to the level of the upper dielectric as shown by Wong for the purpose, for example, to remove excess copper and planarize/polish the copper/dielectric surface (Wong; pp. 1, section [0005], lines 10 – 14).

In re claim 2, 4, and 7, Hsu in view of Hsu and further in view of Wong discloses the methods and device of claims 1, 3, and 6 respectively, wherein the deposition method is PVD (column 6, lines 22-37).

Additionally, such a technique is disclosed by Applicant in the specification to be a "conventional" technique and thus would have been obvious for one of ordinary skill the art at the time of the invention to employ to fabricate the structure.

In re claim 5, Hsu in view of Hsu and further in view of Wong discloses the method of claim 3, wherein the intermediate liner layer comprises Ta/TaN.

Response to Arguments

Applicant's arguments filed 04/06/06 have been fully considered but they are not persuasive.

Applicant's amendments to the claims and remarks directed to are not persuasive in view of the disclose of Hsu ('249) as further expounded by Hsu ('645) to address the additions to the claims brought in by applicant's amendments.

Initially, the arguments addressed to the disclosure of Farrar are not addressed because applicant has successfully amended the claims to take the Farrar disclosure out of consideration.

Therefore, addressing the arguments cited concerning the Hsu ('249) reference, applicant plainly argues that Hsu ('249) does not disclose depositing the aluminum-copper alloy along the sides of a trench and a via. This argument is addressed in the new rejection above, such that the disclosure of Hsu ('249) teaches a damascene interconnect. The secondary reference, Hsu ('645) is included to show that a damascene interconnect is well known to have a trench region as well as a via region.

Second, applicant's comments with regard to the lack of teaching of polishing the copper deposit is not persuasive. Examiner positively addressed claim 6 in the previous rejection regarding the disclosure of Hsu ('249) regarding the desirability of planar layers. In this present rejection, the secondary reference of Hsu ('645) is also consulted to show the desirability of planar layers through the process known as CMP.

Response to Arguments

Applicant's arguments with respect to claims 1 – 7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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